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(54) TITLE OF THE INVENTION

A METHOD OF FABRICATING SEMICONDUCTOR AND SEMICONDUCTOR DEVICE

(57) [ABSTRACT] (Corrected)

[PURPOSE] A method of shortening crystallization time by lowering crystallization temperature of amorphous silicon, and a method of fabricating a thin film transistor by utilizing above mentioned method are provided.

[STRUCTURE] After depositing a base insulating film (ex. silicon oxide film 22), plasma treatment is employed by exposing the base insulating film to a plasma. Then, an amorphous silicon film 22 is deposited, and crystallized at 450-600°C. Moreover, the nucleation sites are controlled by selectively exposing the amorphous silicon film to a plasma atmosphere. By the above method, a portion 26 having good crystallinity is formed at will and a thin film transistor is fabricated by utilizing the portion.

[NAME OF DOCUMENT] Specification

[TITLE OF THE INVENTION] A METHOD OF FABRICATING SEMICONDUCTOR AND FABRICATING SEMICONDUCTOR DEVICE

[CLAIMS]

[CLAIM 1] A process for fabricating a semiconductor comprising the steps of:

forming an insulator coating on a substrate;

exposing said insulator coating to a plasma;

forming an amorphous silicon film on said insulator coating after said exposing step; and

crystallizing said silicon film by processing said silicon film in the temperature range of from 400 to 600°C.

[CLAIM 2] The process for fabricating a semiconductor of claim 1 wherein the substrate is heated in a temperature range of from 100 to 500°C during said exposing step.

[CLAIM 3] The process for fabricating a semiconductor of claim 1 wherein the plasma utilized comprises 10% by volume or more of at least one selected from the group consisting of nitrogen, oxygen, neon, krypton, and argon.

[CLAIM 4] The process of claim 1 wherein said substrate is not exposed to air between said step of exposing an insulator coating to a plasma and said step of forming an amorphous silicon film on said insulator coating.

[ClAIM 5] The process of claim 1 wherein said step of exposing an insulator coating on a substrate to a plasma is carried out in a space provided therein an electrode made of a material containing at

least one element selected from a group consisting of nickel, iron, cobalt, and platinum.

[CLAIM 6] A process for fabricating a semiconductor comprising the steps of:

forming an insulator coating on a substrate;

selectively coating said insulator coating with a masking material;

exposing said substrate to a plasma;

forming an amorphous silicon film on said insulator coating after said exposing step;

crystallizing said silicon film by processing in the temperature range of from 400 to 600°C; and

selectively etching said silicon film.

[CLAIM 7] A process for fabricating a thin film transistor comprising the steps of:

forming an insulator coating on a substrate;

selectively coating said insulator coating with a masking material;

exposing said substrate to a plasma;

forming an amorphous silicon film on said insulator coating after said exposing step;

processing said silicon film in the temperature range of from 400 to 600°C;

selectively etching said silicon film; and

establishing a channel forming region of the thin film transistor out of the portion previously coated with the masking material.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[FIELD FOR INDUSTRIAL USE]

The present invention relates to a process for fabricating a crystalline semiconductor for use in thin film devices such as thin-film insulated-gate field-effect transistors (hereinafter referred to simply as "thin film transistors" or "TFTs").

[0002]

[PRIOR ART]

Thin films of crystalline silicon semiconductor for use in thin film devices such as thin-film insulated-gate field-effect transistors (TFTs) known heretofore have been fabricated by crystallizing an amorphous silicon film formed through plasma CVD (chemical vapor deposition) or thermal CVD, using an apparatus such as an electric furnace at a temperature of not lower than 600°C for a duration of 12 hours of longer. Thin films ~~of crystalline silicon~~ semiconductor having sufficiently high quality ~~(for~~ example, an excellent field effect and a high reliability) are available only after subjecting the amorphous film to a heat treatment for a still longer duration.

[0003]

[PROBLEMS THE PRESENT INVENTION INTENDS TO SOLVE]

However, those prior art processes for obtaining thin films of crystalline silicon semiconductor suffer many problems yet to be solved. One of the problems is the low throughput which increases

the process cost. For instance, if a duration of 24 hours is required for the crystallization step, 720 substrates must be processed at a time considering that preferably, the substrates each consume 2 minutes of process time. However, the maximum number of substrates an ordinary tubular furnace can treat at a time is limited to 50; in a practical treatment using only one apparatus (reaction tube), it has been found that a single substrate consumes 30 minutes to complete the treatment. In other words, at least 15 reaction tubes are necessary to complete the reaction per single substrate in 2 minutes. This signifies an increase in investment cost and therefore an increase of the product price due to a too large depreciation for the investment.

[0004]

The temperature of the heat treatment is another problem to be considered. In general, a TFT is fabricated using a quartz glass substrate comprising pure silicon oxide or an alkali-free borosilicate glass substrate such as the #7059 glass substrate manufactured by Corning Incorporated (hereinafter referred to simply as "Corning #7059"). The former substrate has such an excellent heat resistance that it can be treated in the same manner as in a conventional wafer process for semiconductor integrated circuits. However, it is expensive, and, moreover, the price increases exponentially with increasing the area of the substrate. Thus, at present, the use of quartz glass substrates is limited to TFT integrated circuits having a relatively small area.

[0005]

On the other hand, alkali-free glass is inexpensive as compared to quartz glass, however, it has shortcomings with respect to heat

resistance. Since an alkali-free glass undergoes deformation at a temperature in the range of from 550 to 650°C, and more particularly, since a readily available material initiates its deformation at a temperature not higher than 600°C, any heat treatment at 600°C causes an irreversible shrinkage and warping to form on the substrate. These deformations appear particularly distinctly on a substrate having a diagonal length of more than 10 inches. Accordingly, it is believed requisite to perform the heat treatment on a silicon semiconductor film at a temperature of 550°C or lower and for a duration of within 4 hours to reduce the entire process cost. The present invention is aimed at providing a method of fabricating semiconductor and fabricating semiconductor device filling said requirements.

[0006]

[MEANS TO SOLVE THE PROBLEMS]

The present invention is characterized in that it comprises forming an insulator coating on a substrate; exposing said insulator coating to a plasma; forming an amorphous ~~silicon~~ film on said insulator coating after said process; and processing said silicon film in the temperature range of from 400 to 600°C.

The present invention is further characterized in that it comprises forming an insulator coating on a substrate; selectively coating said insulator film with a masking material; exposing said substrate to a plasma; forming an amorphous silicon film on said insulator coating after said process; processing said silicon film in the temperature range of from 400 to 600°C; and selectively etching said silicon film.

[0007]

Furthermore, the present invention comprises fabricating a thin ilm transistor which is characterized in that it comprises forming n insulator coating on a substrate; selectively coating said nsulator coating with a masking material; exposing said substrate o a plasma; forming an amorphous silicon film on said insulator oating after exposing the substrate to said plasma; processing said ilicon film in the temperature range of from 400 to 600°C; and stablishing a channel forming region of a thin film transistor from he portion previously coated with the masking material.

[0008]

After an extensive study, the present inventors have found a neans for overcoming the aforementioned problems. The present inventors formed a lower insulator layer on a substrate to prevent impurities from intruding into the semiconductor layer from the substrate, and, after once exposing the insulator layer to plasma, deposited a layer of amorphous silicon and thermally crystallized the amorphous silicon. Thus, it has been found that a silicon ~~semiconduc~~tor film deposited on the resulting structure can be crystallized considerably easily.

[0009]

The aforementioned findings can be explained as follows. The reason why a conventional thermal crystallization process at about 600°C requires a long period of time can be explained, in one aspect, by the generation of crystal nuclei which takes a long time. In the present specification, this period of time referred to as a latent period. According to the 24-hour observation of a crystallization process by the present inventors, silicon maintains

its initial amorphous state in the initial period of six hours because no nucleus is formed during this period. In the subsequent period of six hours, nuclei are generated spontaneously, and this step is followed by the crystallization. It can be seen that a prior art process includes a latent period for a duration of from 6 to 12 hours in the entire process time. However, the nuclei thus formed during the latent period are highly disordered, and the concentration of the nuclei differs from place to place. Thus, in particular regions, it happens that the crystallization greatly proceeds; but in other regions, substantially no crystallization is observed to occur. However, with passage of time, nucleation occurs also in those regions in which no nucleation had been observed, or the region of crystallization extends to gradually cover the entire substrate. It can be seen that a period of 12 hours or longer is necessary to obtain a completely crystallized substrate.

[0010]

When the base insulator film is treated with a plasma, a substance which functions as a catalyst for accelerating the crystallization is formed in the insulator film. A catalyst which accelerates the nucleation signifies, for example, a charge or a defect which results from the damage caused by the plasma, or a deposit from a material which constitutes the chamber or the substrate. More specifically, those from materials having a catalytic effect on crystallization, such as nickel, iron, cobalt, and platinum, are found to have marked effects as catalysts. The presence of these catalysts facilitates nucleation and shortens the latent period. Moreover, a larger number of crystal nuclei can be obtained by increasing the amount of these catalysts. This can be assumed by the fact that a longer plasma treatment allows nucleation to occur at a higher density and that it leads to the generation of

finer crystals.

[0011]

Another aspect to be noticed is that the nucleation occurs in an extremely uniform density. This can be confirmed by observing the lightly etched surface of a silicon film crystallized by the present invention. More specifically, the surface of a specimen obtained by deposition on amorphous silicon film on a plasma-treated substrate and thermally treating the resulting structure at 550°C for a duration of 4 hours is observed under an optical microscope, electron microscope, and the like after lightly etching the surface using a fluoronitric acid. Then, it can be found that crater-like minute holes are formed at approximately the same spacing. These holes are believed attributable to the presence of materials liable to be readily etched. In other words, the etched pattern corresponds to the density distribution of crystal nuclei inside the silicon film. It can be assumed that the catalyst is distributed in the same manner as the density (concentration) distribution pattern of the holes.

[0012]

Favorable results on the plasma treatment can be obtained by performing the treatment using a parallel-plate type plasma generation apparatus. Otherwise, the use of a positive column discharge in a chamber while applying a proper bias can also yield favorable results. At any rate, preferred results can be obtained by using an electrode made of nickel, iron, or cobalt for generating the plasma.

Furthermore, the crystallization occurs more easily by heating the substrate to a temperature range of from 100 to 500°C during the

plasma treatment, and more specifically, the substrate is preferably heated to a temperature of 200°C or higher. This is because the catalytic substance can be more readily obtained at higher temperatures.

[0013]

Best results on plasma treatment can be obtained by generating the plasma in an atmosphere containing nitrogen, oxygen, argon, neon, or krypton, and particularly, when these gases are contained in an amount of 10 volume by % or more. The gas is preferably diluted using hydrogen or helium. Moreover, the silicon films which yield the best results were found to be intrinsic or substantially intrinsic, and they were found to contain the foreign elements carbon, oxygen, and nitrogen each at a concentration of 1 X $10^{19}cm^{-3}$ or lower by known secondary ion mass spectroscopy (SIMS).

[0014]

The process according to the present invention comprises plasma treating the surface of a base insulator film. However, when a substrate once subjected to plasma treatment is exposed to the atmosphere, dust, water, and other impurities adhere to the surface to greatly impair the crystallinity of the silicon film. In other words, substrates having a non-uniform characteristics result by the exposure of the substrate to the atmosphere. Such a problem can be circumvented by performing the film deposition and the plasma treatment in a closed system, and maintaining an environment in which the film deposition can be performed continuously without exposing the plasma-treated substrate to air. Furthermore, preferably, the surface of the substrate and the insulating coating is maintained at a sufficiently clean state. For instance, carbon,

organic matter, and the like are preferably removed from the surface by employing ultraviolet irradiation, ozone treatment, or a combination thereof.

[0015]

[EMBODIMENT]

[Embodiment 1] A process for crystallizing a planar amorphous silicon film formed on a Corning #7059 substrate is described below. A 2,000Å thick silicon oxide film was deposited on the substrate as a base film using RF sputtering, and the resulting silicon oxide film was treated in nitrogen plasma. A plasma treating apparatus was of a parallel plane type as shown schematically in Fig.1. Nickel-alloy was utilized for electrodes.

chamber...11, gas inlet system...12,
evacuation system...13, RF power source...14,
electrodes 15,16, substrate...17,
RF plasma...18

[0016]

Condition of the plasma treatment was as the following:

RF power.....20W or 60W
Reactive gas.....nitrogen (flow rate of 100SCCM)
Reaction time.....5 minutes
Substrate temperature....200°C
Reaction pressure.....10Pa (where, a vacuum degree of 10^{-3} Pa or lower is achieved)

[0017]

Then, a 1,500Å thick amorphous silicon film was deposited by plasma CVD, and after removing hydrogen from the film by keeping it at a temperature of 430°C for 1 hour, solid phase growth was allowed to take place thereon in the temperature range of from 500 to 580°C for a duration of from 10 minutes to 8 hours.

[0018]

The above steps may be performed otherwise using, for example, an apparatus having two or more chambers as shown in Fig.5, so that the steps can be performed continuously. Particularly, the above processes comprise depositing the amorphous silicon film after once exposing the plasma-treated silicon oxide base to air. The process according to the present invention is sensitive to the surface conditions, and the characteristics of the resulting crystalline silicon film tend to be greatly influenced by the inclusions which may adhere to the surface of the substrate during its exposure to air.

[0019]

Referring briefly to the apparatus illustrated in Fig.5, it comprises a chamber 501 which is a sputtering apparatus, and a plasma is generated by supplying electric power to two electrodes (sample holder) 502 and (a backing plate) 503 from an RF power source 504. A substrate 506, which is the sample, and a target 505 are placed on the respective electrodes. This target in this case is silicon oxide. This chamber is further equipped with a gas system 507 for introducing a gas mixture comprising oxygen gas and argon gas, and another gas system 508 for introducing nitrogen gas. Thus, a gas is supplied from the former system during the deposition of the silicon oxide film, and during the plasma treatment, the gas

is supplied from the latter system. 509 is an evacuation system.

[0020]

A chamber 521 is a parallel plane type plasma CVD apparatus. A plasma can be generated by supplying an electric power from an RF power source 524 to two electrodes 522 and 523. A sample substrate 525 is mounted on the electrode 522. A gas system 526 introducing a gas mixture of silane and hydrogen is provided to this chamber, and a film formed by plasma reaction is formed on the substrate 525. Though not shown in the figure, a mechanism is provided to those chambers as such that the substrate can be heated to a proper temperature.

An additional chamber 510, in which a substrate 511 is placed, is provided between the two plasma chambers.

[0021]

In a process using the apparatus illustrated in Fig.5, nitrogen plasma treatment is performed immediately after the completion of silicon oxide film deposition using sputtering in the chamber 501, by replacing the atmosphere inside the chamber with nitrogen. If a silicon oxide target should remain inside the chamber, further deposition of silicon oxide film occurs by sputtering. To prevent this from occurring, the RF power must be lowered or the silicon oxide target must be isolated from the plasma. Fortunately, as described hereinafter, plasma treatment is performed optimally at a power of 60W or lower, and preferably, at a power of 20W, as compared with an RF power of 100W or higher required for sputtering. Accordingly, no deposition of silicon oxide occurred during the treatment in nitrogen plasma. To further assure the process, however, a chamber for depositing the silicon oxide film is

preferably installed separately from the chamber for use in plasma treatment. An amorphous silicon film thus deposited was also subjected to solid-phase crystallization under the same conditions described hereinbefore.

[0022]

After allowing the amorphous silicon film to undergo solid phase crystal growth, the degree of crystallization thereof was evaluated using Ar^+-laser Raman spectroscopy. The results are shown in Figs. 6 and 7. The ordinate in both of the graphs represents relative intensity taking the Raman peak intensity of a standard sample (a single crystal silicon) as unity. It can be read from the graphs that no crystallization occurs by heat treating a sample without plasma treatment at 580°C or lower for a duration of 8 hours or less. In contrast to this, both of the samples plasma-treated at an RF power of 20W and 60W are found to undergo crystallization.

[0023]

With a careful inspection of the results, it can be seen that the crystallization proceeds as a function of the RF power. More specifically, the crystallization proceeds rather sluggishly under a low power (20W). At least an annealing for a duration of 1 hour is necessary to crystallize the amorphous silicon film at 550°C. In other words, the latent period is 1 hour. However, after the passage of an hour, the crystallization proceeds swiftly to attain a saturated state within 2 hours of annealing. By comparing the Raman peak intensity, it can be seen that a crystallization degree well comparable with that of a standard sample, i.e., a single crystal silicon, is achieved for the sample after the annealing of 2 hours.

[0024]

In contrast to the case above, crystallization proceeds relatively swiftly under a high RF power (60W). For example, an annealing for 4 hours allows the amorphous silicon film to crystallize at a temperature as low as 480°C, and by increasing the temperature to 550°C, an annealing for a duration of mere 10 minutes (i.e., a latent period of 10 minutes) initiates crystallization and achieves a saturated state in an hour. However, the degree of crystallization is low, and the Raman intensity only corresponds to less than 70% of that obtained for a silicon film crystallized under a low power (20W).

[0025]

This difference can be explained in terms of the nucleation density. That is, nuclei are generated at a low density when the plasma treatment is applied under a low power condition, because the concentration of the catalytic substance is low. Thus, the crystallization of these nuclei requires a treatment at a high temperature and a long duration. However, the resulting crystallites have high crystallinity and yield a high Raman intensity ratio. On the other hand, catalytic substances are generated at a high concentration by applying a plasma treatment under a condition of high power. Since nucleation occurs at high density, crystallization occurs relatively easily. However, the nuclei interfere each other during their growth, and the film which is obtained as a result has a poor crystallinity.

At any rate, the application of a plasma treatment enables crystallization to take place at a low temperature and within a short period of time as compared with the case with no plasma treatment. Obviously, the crystallization at a low temperature and

in a short period of time is achieved by applying a plasma treatment. In the present Embodiment, the concentration of the catalytic substance was controlled by controlling the RF power, however, other factors, such as the pressure applied during the plasma treatment, the type and the component of gas, the temperature of the sample, and the duration of processing, are all important factors for controlling the concentration of the catalytic substance.

[0026]

[Embodiment 2]

A process for selectively crystallizing by selectively treating the base oxide film using a plasma treatment is described below. Referring to Fig.2, a 2,000Å thick silicon oxide film 22 was deposited as a base on a Corning #7059 substrate 21 by sputtering, and a heat-resistant photoresist 24 was applied thereon by spin-coating. After patterning the resulting photoresist film 24, the entire substrate was exposed to nitrogen plasma in the same manner as in Embodiment 1 to perform plasma treatment on the exposed portion 23 of the oxide film base. The plasma treatment was effected under the same conditions as those employed in Embodiment 1, except for setting the RF power to 60W. thus was obtained a structure shown in Fig.2(A).

[0027]

Since the substrate at this point is heated to a temperature of 200°C or higher, the masking material to be used herein must at least resist to the same temperature. Furthermore, preferably, the masking material is removable without using a plasma. Thus, the use

of a heat-resistant photoresist for the mask is preferred from these points of view. Otherwise, inorganic materials such as titanium nitride, silicon oxide, and silicon nitride can be used as well.

[0028]

Subsequently, an annealing at 550°C for a duration of 4 hours is performed after depositing a 1,500Å thick amorphous silicon film 25 by low pressure CVD. As a result, crystalline silicon 26 was observed to be formed around the portions remained uncovered by the masking material on plasma treatment before. The crystallization extended into portions covered by the masking material (but only portions treated by the plasma) for about 5 μm along the longitudinal direction. No crystallization was observed to occur on other portions covered by the masking material.

[0029]

Noticeably, the crystallinity for the peripheral portions at a distance of 5 μm from those plasma-treated portions was better than that of the portions subjected to plasma treatment. In the former, the crystallites initiate growth from a plurality of independent nuclei, and that then they collide with each other to interfere their growth. On the other hand, the latter contain no nucleus, and the direction of crystal growth is confined to a single direction. It can be seen that the crystal growth is allowed to take place without any limitations.

[0030]

[Embodiment 3]

A process for fabricating a TFT having particularly high mobility by selectively performing a plasma treatment is described below. More specifically, the masking material was formed only on a portion for fabricating a channel forming region (i.e., a region located under the gate electrode and between a source and a drain in an island-like semiconductor region) of a TFT to prevent this portion from being exposed to plasma. However, since crystallization proceeds, though depending on the annealing temperature and duration, in a region from several micrometers to ten micrometers in size as described in the foregoing Embodiment 2, this process is not suitable for a device having to long a channel length and too wide a channel width.

[0031]

In the plasma treatment, the surface of the silicon oxide base is subject to defects due to the impact exerted by the plasma. Moreover, various types of foreign matter adhere to the surface. A part of these defects and foreign matter functions as a catalyst to accelerate nucleation, however, it also may cause leak current if it is found in the channel forming region of a TFT. Furthermore, a TFT having high mobility can be obtained only by using semiconductors of high crystallinity. Thus, by referring to Embodiment 2 above, the peripheral portions are preferred to the plasma treated portions in this case. Referring to Fig.3, the process according to the present embodiment is described below.

[0032]

A 2,000Å thick silicon oxide film 31 was deposited as a base on a Corning #7059 substrate 30 by sputtering, and a heat-resistant photoresist was applied thereon to form masks 32A and 32B each at

the same size as the channel, i.e., 5 μm x 15 μm. Otherwise, the mask can be patterned using the patterning for the gate connection, because, as described hereinafter, the effect is the same for both considering the amorphous silicon film. The resulting substrate was placed into a plasma 33 to perform the plasma treatment as shown in Fig.3(A). The same plasma treating apparatus as that used in Embodiment 1 was used. The process condition is as the following:

RF power	60W
Reactive gas	nitrogen (flow rate of 100SCCM)
Reaction time	5 minutes
Substrate temperature	200°C
Reaction pressure	10Pa (a vacuum degree of 10^{-3} Pa or lower is achieved)

[0033]

The masks 32A and 32B were removed after the plasma treatment, and a 1,500Å thick amorphous silicon film was deposited thereon by low pressure CVD using monosilane (SiH_4) as the material gas. Subsequently, annealing was effected at 550°C for a duration of 4 hours to allow the film to crystallize. The thus crystallized film was patterned to form island-like silicon regions 34A and 34B, and this was followed by the deposition of a 1,000Å thick silicon oxide film 35 by plasma CVD using tetraethoxysilane (TEOS) and oxygen as the material gases. After depositing an N-type polysilicon film by low pressure CVD, the resulting structure was subjected to patterning to form a gate connection electrodes 36A and 36B (Fig.3(B)).

[0034]

Then, impurity doping was performed using plasma doping. In

this case, phosphine (PH_3) and diborane (B_2H_6) were used as the N-type and P-type impurity sources, respectively. Phosphine was doped by applying an accelerating voltage of 80keV, and diborane was doped under a voltage of 65keV. The impurity region 37 was formed by further annealing the structure at 550°C for 4 hours to activate the impurities. This activation can be performed by a method using an optical energy, such as laser annealing and flash lamp annealing (Fig.3(C)).

[0035]

Finally, a 5,000Å thick silicon oxide film was deposited as an interlayer insulator 38 in the same manner as in an ordinary process for fabricating a TFT. By forming contact holes, connection contacts 39A and 39B were formed in the source region and the drain region (Fig.3(D)).

The final structure of the TFT circuit as viewed from the upper side is given in Fig.3(E). The cross section views in Figs. 3(A) to 3(D) are taken along the dashed line drawn in Fig.3(E). The TFT thus obtained was found to have a field-effect mobility of from 40 to 60 cm^2/Vs in the N-channel type, and of from 30 to 50 cm^2/Vs in the P-channel type.

[0036]

[Embodiment 4]

This embodiment is a process for fabricating an aluminum-gate TFT according to the present invention. Fig.4 shows the process of this embodiment.

A base film 41 (2,000Å thickness) of silicon oxide is formed on a substrate (Corning 7059) 40 by sputtering. The substrate was

exposed to plasma 42, and plasma treatment was performed as shown in Fig.4(A). The plasma treatment apparatus utilized was the same apparatus as that of Embodiment 1. Process condition was as the following:

RF power	20W
Reactive gas	argon (flow rate of 100SCCM)
Reaction time	5 minutes
Substrate temperature	200°C
Reaction pressure	10Pa (a vacuum degree of 10^{-3} Pa or lower is achieved)

[0037]

Then, a 1,500Å thick amorphous silicon film 43 was deposited thereon by low pressure CVD using monosilane (SiH_4) as the material gas. Subsequently, annealing was effected at 550°C for a duration of 4 hours to allow the film to crystallize. (Fig.4(B))

The thus crystallized film was patterned to form an island-like silicon region 44, and this was followed by the deposition of a 1,000Å thick silicon oxide film 45 by plasma CVD using tetraethoxysilane (TEOS) and oxygen as the material gases. After depositing a 5,000Å thick aluminum film containing 1% of silicon by sputtering, the aluminum film was patterned to form a gate connection·contact 46. (Fig.4(C))

[0038]

Subsequently, the substrate was subjected to anodic oxidation by dipping it into an ethylene glycol solution containing 3% of tartaric acid and applying current between a platinum cathode and the aluminum connection 46 (anode). The current was applied in such

manner that the voltage thereof would increase in the initial state at a rate of 2 V/minute, and that a constant voltage is maintained after a voltage of 220V is attained. The current was turned off at the point the current dropped to 10 μA/m² or lower. Thus was obtained a 2,000Å thick anodic oxide 47 as shown in Fig.4(D).

[0039]

Then, impurities were introduced using plasma doping. In this case, phosphine (PH_3) and diborane (B_2H_6) was used as the N-type and P-type, respectively. Accelerating voltage was 80 keV for phosphine, and 65 keV for diborane. The impurity region 48 was formed by further laser annealing the structure applying 5 shots using a KrF excimer laser operating at a wavelength of 248 nm and emitting a laser beam at an energy density of from 250 to 300 mJ/cm². The resulting structure is shown in Fig.4(E).

[0040]

Finally, a 5,000Å thick silicon oxide film was deposited as an interlayer insulator 49 in the same manner as in an ordinary process for fabricating a TFT. By forming contact holes in the resulting silicon oxide film, connection contacts 50A and 50B were formed in the source region and the drain region (Fig.3(F)).

The TFT thus obtained was found to have a field-effect mobility of from 40 to 60 cm²/Vs in the N-channel type, and of from 30 to 50 cm²/Vs in the P-channel type. Furthermore, a shift resistor fabricated using this TFT was observed to operate at 6 MHz with a drain voltage of 17V, and at 11 MHz with a drain voltage of 20V.

[0041]

[EFFECT OF THE PRESENT INVENTION]

As described in the foregoing, the present invention is epoch-making in that it enables the crystallization of an amorphous silicon to take place at an even lower temperature and within a shorter period of time. Furthermore, the process according to the present invention is suitable for mass production, and yet, it can be performed employing the most commonly used equipments, apparatuses, and methods. Accordingly, it is a promising and a beneficial process for the electronic industry.

[0042]

More specifically, for instance, a conventional solid phase growth process requires an annealing step for a duration of at least 24 hours. Considering that the process time per substrate is preferably 2 minutes, 15 annealing furnaces are necessary to make the process practically feasible. However, the present invention allows the process to complete within 8 hours, and under optimal conditions, the process can be even more shortened to a mere 4 hours or less. This signifies that the process can be performed while reducing the number of furnaces to only a sixth or less of the above calculated number. This leads to an increase of productivity and the cutting down of equipment investment, thereby lowering the process cost of the substrates. Accordingly, economical TFTs can be produced, and this might call novel demands. Conclusively, the present invention is greatly beneficial for the industry.

[BRIEF EXPLANATION OF FIGURES]

[Fig.1] This shows an apparatus for performing a process

according to an embodiment of the present invention. (see Embodiment 1)

[Fig.2] This shows process of Embodiment 2. (selective crystallization)

[Fig.3] This shows a figure of manufacturing process of TFT according to Embodiment 3 (cross section).

[Fig.4] This shows a figure of manufacturing process of TFT according to Embodiment 4 (cross section).

[Fig.5] This shows an Embodiment of the apparatus embodying the present invention (see Embodiment 1)

[Fig.6] This shows the change of Raman scattering intensity ratio with the duration of annealing observed on a silicon film obtained in Embodiment 1, in which the intensity ratio signifies the relative intensity taking the Raman scattering intensity of a standard sample (single crystal silicon) as unity.

[Fig.7] This shows the change of Raman scattering intensity ratio with changing temperature of annealing observed on a silicon film obtained in Embodiment 1, in which the intensity ratio signifies the relative intensity taking the Raman scattering intensity of a standard sample (single crystal silicon) as unity.

[Explanation of marks]

11...chamber
12...gas inlet system
13...evacuation system
14...RF power source
15,16...electrode
17...substrate (sample)

18...RF plasma

21...substrate

22...base silicon oxide film

23...plasma treated surface

24...mask material

25...amorphous silicon film

26...crystallized silicon film

27...non-crystallized silicon film

30...substrate

31...base silicon oxide film

32...mask material

33...plasma

34...crystal silicon region

35...gate insulating film (silicon oxide)

36...gate electrode (N silicon)

37...impurity region(source, drain)

38...interlayer insulator

39...source electrode

drain electrode

40...substrate

41...base silicon oxide film

42...plasma

43...amorphous silicon region

44...crystal silicon region

45...gate insulating film (silicon oxide)

46...gate electrode (aluminum)

47...anodic oxide (aluminum oxide)

48...impurity region(source,drain)

49...interlayer insulator

50...source electrode

drain electrode

501...sputter chamber

502...electrode(sample side)

503...electrode (target side)

504...RF power source

505...target

506...sample (substrate)

507...gas (oxygen/Ar) system

508...gas (nitrogen) system

509...evacuation system

510...additional chamber

511...sample (substrate)

521...plasma CVD chamber

522...electrode (sample side)

523...electrode (countering)

524...RF source

525...sample (substrate)

526...gas (silane/hydrogen) system

527...evacuation system

[NAME OF DOCUMENT] Abstract

[ABSTRACT]

[PURPOSE] A method of shortening crystallization time by lowering crystallization temperature of amorphous silicon, and a method of utilizing a thin film transistor by utilizing above mentioned method are provided.

[STRUCTURE] After depositing a base insulating film (such as a silicon oxide film), plasma treatment is employed by exposing the base insulating film to a plasma. After that, an amorphous silicon film is deposited, and is crystallized at 450 to 600°C. The nucleation sites are controlled by selectively exposing the amorphous silicon film to a plasma or by selectively applying a substance containing elements having a catalytic effect thereto. A process for fabricating a thin film transistor using the same is also disclosed.

[SELECTED FIGURE] Fig.3

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